WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

a gate insulating film and a gate electrode formed on said semiconductor substrate;

a pair of first sidewall insulating films formed on the lateral portions of said gate electrode;

a pair of second sidewall insulating films formed so as to sandwich said first sidewall insulating films with said gate electrode, and having a width larger than that of said first sidewall insulating films;

a pair of first N-type impurity-diffused layers containing phosphorus formed in the surficial portion of said semiconductor substrate at a first depth so as to be self-aligned with respect to said gate electrode and said first sidewall insulating films;

a pair of second N-type impurity-diffused layers formed in the surficial portion of said semiconductor substrate at a second depth deeper than said first depth so as to be self-aligned with respect to said gate electrode, said first sidewall insulating films and said second sidewall insulating films; and

a pair of P-type impurity-diffused layers formed between said pair of second N-type impurity-diffused layers, and respectively in adjacent to each of said pair of first N-type impurity-diffused layers.

2. The semiconductor device according to claim 1, wherein said first sidewall insulating films have a thickness of 5 to 15 nm.

3. The semiconductor device according to claim 1, wherein said first N-type impurity-diffused layers contain arsenic.

4. The semiconductor device according to claim 1, wherein phosphorus accounts for 50 atomic percent or more of N-type impurities introduced into said first N-type impurity-diffused layers.

5. A semiconductor device comprising:

a semiconductor substrate;

a gate insulating film and a gate electrode formed on said semiconductor substrate;

a pair of sidewall insulating films formed on the lateral portions of said gate electrode;

a pair of first P-type impurity-diffused layers formed in the surficial portion of said semiconductor substrate at a first depth so as to be self-aligned with respect to said gate electrode;

a pair of second P-type impurity-diffused layers formed in the surficial portion of said semiconductor substrate at a second depth deeper than said first depth so as to be self-aligned with respect to said gate electrode and said sidewall insulating films; and

a pair of N-type impurity-diffused layers containing phosphorus formed between said pair of second P-type impurity-diffused layers, and respectively in adjacent to each of said pair of first P-type impurity-diffused layers.

6. The semiconductor device according to claim 5, wherein said N-type impurity-diffused layers contain arsenic.

7. The semiconductor device according to claim 5, wherein phosphorus accounts for 30 atomic percent or more

of N-type impurities introduced into said N-type impurity-diffused layers.

8. The semiconductor device according to claim 1, wherein the length of said gate electrode is not longer than 100 nm.

9. The semiconductor device according to claim 5, wherein the length of said gate electrode is not longer than 100 nm.

10. A method of fabricating a semiconductor device comprising the steps of:

forming a gate insulating film and a gate electrode on a semiconductor substrate;

forming a pair of P-type impurity-diffused layers by introducing a P-type impurity into the surficial portion of said semiconductor substrate with using said gate electrode as a mask;

forming a pair of first sidewall insulating films on the lateral portions of said gate electrode;

forming a pair of first N-type impurity-diffused layers at a first depth by introducing at least phosphorus into the surficial portion of said semiconductor substrate with using said gate electrode and said first sidewall insulating films as a mask;

forming a pair of second sidewall insulating films so as to sandwich the said first sidewall insulating films with said gate electrode, and so as to have a width larger than that of said first sidewall insulating films; and

forming a pair of second N-type impurity-diffused layers at a second depth deeper than said first depth by introducing an N-type impurity into the surficial portion of said semiconductor substrate with using said gate

electrode, said first sidewall insulating films and said second sidewall insulating films as a mask.

11. The method of fabricating a semiconductor device according to claim 10, wherein said first sidewall insulating films are formed to a thickness of 5 to 15 nm.

12. The method of fabricating a semiconductor device according to claim 10, wherein in said step of forming a pair of first N-type impurity-diffused layers, arsenic is introduced together with phosphorus into the surficial portion of said semiconductor substrate.

13. The method of fabricating a semiconductor device according to claim 10, wherein said first N-type impurity-diffused layers are adjusted so that phosphorus accounts for 50 atomic percent or more of the N-type impurities introduced therein.

14. A method of fabricating a semiconductor device comprising the steps of:

forming a gate insulating film and a gate electrode on a semiconductor substrate;

forming a pair of N-type impurity-diffused layers by introducing at least phosphorus into the surficial portion of said semiconductor substrate with using said gate electrode as a mask;

forming a pair of first P-type impurity-diffused layers at a first depth by introducing a P-type impurity into the surficial portion of said semiconductor substrate with using said gate electrode as a mask;

forming a pair of sidewall insulating films on the lateral portions of said gate electrode; and

forming a pair of second P-type impurity-diffused layers at a second depth deeper than said first depth by

introducing a P-type impurity into the surficial portion of said semiconductor substrate with using said gate electrode and said sidewall insulating films as a mask.

15. The method of fabricating a semiconductor device according to claim 14, wherein in said step of forming a pair of N-type impurity-diffused layers, arsenic is introduced together with phosphorus into the surficial portion of said semiconductor substrate.

16. The method of fabricating a semiconductor device according to claim 14, wherein said N-type impurity-diffused layers are adjusted so that phosphorus accounts for 30 atomic percent or more of the N-type impurities introduced therein.

17. The method of fabricating a semiconductor device according to claim 10, wherein in said step of forming a gate electrode, said gate electrode is formed to a length of not longer than 100 nm.

18. The method of fabricating a semiconductor device according to claim 14, wherein in said step of forming a gate electrode, said gate electrode is formed to a length of not longer than 100 nm.